Jaythan Dao

408-718-8689 | jaythan.dao@berkeley.edu | linkedin.com/in/jaythan-dao | github.com/jt-dao |

Education

University of California, Berkeley B.S. Graduation - May 2027

Electrical Engineering and Computer Science (EECS)
Coursework: Graduate Digital ICs & Systems, Design Automation (DV/FV), Digital Design & ICs (FPGA/ASIC Lab), Computer Architecture, Microelectronic Circuits, Machine Learning, Discrete Math & Probability
Languages: SystemVerilog, Verilog, Python, C/C++, Tcl, RISC-V Assembly
Tools: AMD Vivado, Synopsys (VCS, Verdi), Cadence (JasperGold, Innovus, Xcelium, Genus)
Skills: RTL Design, Formal Verification, SystemVerilog Assertions, Microarchitecture, Static Timing Analysis, Synthesis

Digital Design Projects

USB2 PHY Verification + Integration | *Chisel, Verilog* Mar. 2026 – May 2026

- Built a Chisel behavioral verification environment targeting the USB2 PHY ULPI boundary on SkyWater 130nm.
- Modeled and tested packet ID types (Token, Data, Handshake, Special) and DATA0/DATA1 toggle-bit logic.
- Integrated analog, clock recovery, and digital logic subsystems into an end-to-end system with a unified testbench.

RISC-V CPU ASIC Implementation | *SystemVerilog* Mar. 2026 – May 2026

- Adapted 3-stage RISC-V core for SKY130 ASIC implementation with synchronous SRAMs, direct-mapped caches.
- Designed write-through cache control with ready/valid handshakes and request tracking to prevent duplicates.
- Executed synthesis, floorplanning, and place & route; refined SRAM placement, routing, and power-grid geometry.
- Optimized cache-hit latency and throughput through parallel tag/data reads and pipelined requests.
- Traced the SRAM-to-PC critical path through cache and branch-control logic; achieved 87ps post-route slack.

RISC-V CPU on FPGA | *Verilog, C* Oct. 2025 – Dec. 2025

- Built a 3-stage pipelined RISC-V processor supporting RV32I ISA from scratch in Verilog.
- Synthesized and deployed the processor on a Xilinx FPGA with memory-mapped UART for on-board debugging.
- Implemented forwarding, hazard control, and pipeline flushes to handle data dependencies and branch redirects.
- Verified RTL with Verilog testbenches and SystemVerilog assertions; debugged with Icarus Verilog and GTKWave.
- Implemented backward-taken, forward-not-taken branch prediction and predecoding, targeting critical path logic.

Experience

SpaceX May 2026 – August 2026

Software Engineer Intern Hawthorne, CA

- Flight software, embedded development, and hardware-in-the-loop testing for mission-critical vehicle electronics.
- Debugged FPGA Ethernet MAC, PCS, and GTY registers to resolve an eight-month retimer link polarity issue.
- Built datapath rerouting system that restores hardware functionality around a formerly fatal orbital vulnerability.
- Brought up phased-array hardware and built telemetry firmware to monitor component health across the array.
- Developed end-to-end fault detection and recovery logic to handle thermal conditions across flight and ground.
- Integrated CI/CD into live in-orbit software repo to automate build, test, and deployment of software updates.

ASML May 2025 – August 2025

Hardware Engineer Intern San Jose, CA

- Developed projects for the Reliability Lab to enhance hardware testing workflows and performance validation.
- Integrated 9 tests profiles into a Python/Tk GUI for multi-band spectrum analyzer control with trigger activation.
- Controlled lab instruments via GPIB/PyVISA with custom span, sample rate/step, frequency window, resolution.
- Wrote Assembly SPI protocol routine to upgrade programmable digital trimmer from 8- to 10-bit resolution.
- Designed evaluation circuits in OrCad and derived op-amp gains to validate digital potentiometer outputs.

Biomimetic Millisystems Lab Jan. 2025 – Present

Electrical Engineer Researcher UC Berkeley / Berkeley, CA

- Designed a 2-layer PCB (250+ components) for endonasal surgical robot evaluation in collaboration with UCSF.
- Ran PCB bring-up & rework, diagnosing and resolving power, signal, and firmware issues for first-pass validation.
- Built mixed-signal power system with parallel buck converters, 32-ch DAC, and 16-ch ADC sensor readback.
- Automated validation of 32+ pressure regulators, sensors, solenoids, motor controllers to cut test time by 15%.
- Developed microcontroller (STM32) firmware supporting I2C, SPI, and serial communication for board testing.

UL Solutions May 2024 – July 2024

Consumer Technologies Intern Fremont, CA

- Utilized Python scripts and operated robotic equipment to evaluate wireless transmission of client electronics.
- Tested to uphold FCC/ICC standards; ensured compliance by analyzing data and running checks on SAR liquids.